DANIEL RUDOLF

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EDUCATION

FLORIDA INSTITUTE OF TECHNOLOGY
Master of Science Computer Engineering, June 1990
Bachelor of Science Electrical Engineering, June 1986

EXPERIENCE

SAPPHIRE COMPUTERS, INC., YELLOW SPRINGS, OH
President, February 1996 to Present
Scope: Consulting in high-speed digital design specializing in FPGA, microprocessor and microcontroller design from small cores to entire systems. Sapphire Computers, Inc. is a Xilinx Alliance partner.

CONTRACTS:

- ***January 2012 to present –*** **Advatech Pacific**, San Bernardino, CA: Presently designing a man wearable version of the Tactical Cross Domain Solution (TACDS – see below) to allow battery operation and provide all the functionality of a Cross Domain Solution (CDS) in a much reduced size and power.
- ***October 2011 to present –*** **Ohio State University**, Columbus OH: Implemented a customer supplied DSP algorithm in VHDL targeting Xilinx FPGA implementation. A full simulation and correlation a Matlab model was done and then the verified design is implemented in a Virtex-6 LX240T.
- ***September 2010 to November 2011 –*** **Advatech Pacific**, San Bernardino, CA: Lead board designer for the Tactical Cross Domain Solution (TACDS) which provides automated cross domain solution (CDS) that executes user programmable rule sets. This design implements a triple processor system with dual Ethernet, USB, serial and adds the capability of Wi-Fi all in a small, low power, hardened form factor that meets Mil STD 1275 electrical specifications. In aggressive program we went from idea to fully functional prototypes in four months.
- ***March 2000 to present –*** **Air Force Research Lab Anti-Tamper/Software Protection Initiative (AT-SPI)**, Dayton, OH: Lead design engineer providing hardware design and FPGA design support for the AT-SPI initiative from its' inception.
- ***March 2010 to July 2010 –*** **Naval Research Labs**, Washington DC: Implemented a stand alone hardened SRAM test unit for radiation testing and verification. Multiple Xilinx Picoblaze processors drive different test patters, verify results and display them on an LCD display. This is implemented in a Xilinx Spartan 3A FPGA.
- ***July 2010 to September 2010 –*** **Old Bird Inc.**, Cornell, NY: Designed a high quality audio preamp for automatic identification of bird calls of migrating birds. Added lighting protection to the system and an hourly calibration tone implemented in a PIC microcontroller.
- ***January 2009 to March 2010 –*** **Naval Research Labs**, Washington DC: Implemented a hardened SRAM test fixture for radiation testing and verification. This is implemented in a Xilinx Spartan 3 1000 FPGA.
- ***December 2008 to January 2009 –*** **Silver Engineering**, Melbourne, FL: Provided a backend interface in VHDL for the Xilinx PCI core providing master and slave bursting capability. Implemented in a Xilinx Spartan-3 FPGA.
- ***May 2008 to December 2008 –*** **Northrop Grumman Corp.**, Dayton, OH: Sentinel-XD card. This Virtex 4 based PMC card utilizes Xilinx's "*Single Chip Crypto"* solution. The board has three banks of DDR2 SDRAM and is designed for a rugged, high temperature environment. Also designed and delivered a Carrier Card that powered the Sentinel-XD card for use in a military vehicle.
- ***September 2006 to August 2008, support on-going –*** **University of Kentucky**, Lexington, KY: Designed a custom video processing board. This board takes 4 HDMI video inputs, implements custom real time video processing on the video streams and then outputs the result over 4 HDMI outputs. This board implements all the processing in a Virtex 4 FPGA with 4 independent banks of SDRAM. The FPGA design was written in VHDL and debugged utilizing a full simulation testbench. The board has a USB interface for setup and control and a SD card interface for data storage.
- ***March 2006 to August 2006 –*** **Northrop Grumman Corp.**, Dayton, OH: Designed a flight hardened Ethernet interface card. This included a Xilinx Spartan-3 1000 FPGA and dual Ethernet MAC/PHYs on a Compact PCI mezzanine card. The board is conductively cooled with a thermal core.
- ***October 2005 to June 2006 –*** **LaserLinc Inc.**, Yellow Springs, OH: Designed an Analog Devices Blackfin DSP processor board to do real time processing on data from ultrasonic thickness gauge. This card also contains SDRAM, Flash, Ethernet and a Xilinx 2S400e FPGA.

- ***September 2004 to August 2005 –*** **Northrop Grumman Corp.**, Dayton, OH/ **ITT**, Denver, CO: Phase 2 of Cyber Channel Card is a XC2VP40 based 64bit/66MHZ PCI card that interfaces to an obsolete super computer system. This card has four 2.5GHZ Fiber Gigabit I/O ports, a 10/100 Ethernet port and 4 Meg of DDR SDRAM.
- ***October 2004 to February 2005 –*** **A_**, (Name withheld due to NDA): System design for a PCI Express fiber optic bus extender. Includes custom FPGA interfaces.
- ***May 2003 to October 2003 –*** **Nothrup Grumman Corp.**, Dayton, OH: Designed, built and delivered 16 Cyber Channel Cards. This is a XC2V3000 based 64bit/66MHZ PCI card that interfaces to an obsolete super computer system and includes a 160 conductor parallel interface running at 133MHZ. This 10 layer impedance controlled card also contains 4 Meg of synchronous SRAM.
- ***February 2003 to November 2003 –*** **MTL Systems Inc.**, Beavercreek, OH: Designed, built and delivered 12 32-bit PCI cards that take video data from a USB 2 video camera and implements a proprietary real-time image processing algorithm in hardware.
- ***July 2003 to October 2003 –*** **Systran Corp.**, Dayton, OH: Modified Xilinx VHDL DDR SDRAM application design and customized it to customer's application. Included user interface to the design and making the design work at 125Mhz/250Mhz.
- ***January 2002 to June 2002 –*** **Silver Engineering**, Melbourne, FL: IMAGE Program. Provided space based reconfigurable computing design analysis of the possibilities of using partial reconfiguration in Xilinx FPGAs for space applications.
- ***December 2001 to February 2002 –*** **A_**, (Name withheld due to NDA): Designed a USB interface to user supplied logic. Includes a Virtex II 1000 interface and board design.
- ***July 2001 to March 2002 –*** **Telesuite Inc.**, Dayton, OH: Worked with customer defining a next generation video CODEC for a very high-end video conferencing system. This is a multiprocessor CompactPCI system with custom hardware color space conversion, integrated scalers and DSP implemented H.26L video encoding.
- ***July 2001 to February 2002 –*** **Synthetic Blood International**, Dayton, OH: Designed an implantable glucose monitor. This high-integration low-power design consists of a microcontroller, RF link, serial EEPROM and A/D conditioning components all in a 1" square by 1/4" form factor. Also designed and built test equipment for the host part of the RF interface.
- ***February 2001 to May 2001 –*** **IBM Microelectronics**, Burlington, VT: Helped implement a custom test board for first-silicon functional/timing test of IBM next generation PowerPC processors. Implemented design in VHDL using Synplify Pro in a Virtex 1000E. Responsibility included implementation of full board test bench and entire V1000 design.
- ***March 2000 to June 2002, support/enhancements ongoing*** A_, (Name withheld due to NDA): Implemented PCI core in SpartanII to provide the interface to battery backed up customer supplied logic. Included entire PCI board design and FPGA with target-only FPGA design.
- ***May 2000 to December 2000–*** **TLA Inc.**, Yellow Springs OH: Implemented PCI core in SpartanII to interface to a laser scanner micrometer. Tasks included entire PCI board design and FPGA with FIFO design to interface with scanner.
- ***February 2000 to March 2002 –*** **Systran Federal Systems**, Dayton OH: Responsible for hardware design for Xilinx FPGA based Reconfigurable Computer. This SBIR (Phase I and Phase II) grant project demonstrates reconfigurable computing and provides a next generation RC platform for accelerating digital signal processing applications. Co-author of a patent for an ultra-flexible reconfigurable computer architecture, pending.
- ***September 1999 to June 2000*** – **Naval Research Labs**, Washington DC: Redesigned the CPU for the NEMO ultra-spectrum satellite. Work involved increasing speed and adding functionality to the present PowerPC 603 design and verifying space ready timing and design.
- ***November 1998 to July 2000*** – **Naval Research Labs**, Washington DC: Designed the prototype Tower CPU (TCPU) board for the GLAST (Gamma-ray Large Area Space Telescope). This satellite will be used to provide astronomers and physicists a direct view of galactic gamma-ray sources such as neutron stars, black holes and blazars. The TPCU VME board is a 64-bit PowerPC board with a level 2 cache, 256 Meg of Reed-Solomon error corrected DRAM, Ethernet, Flash and dual UARTs. The Reed-Solomon error correction, DMA, interrupt and cache control circuitry is all custom designed in 130,000 gates of FPGA. The TCPU board has power and clock frequency control.
- ***February 1999 to September 1999*** - **Scitex Digital Printing**, Dayton OH: Designed and implemented a frame grabber and print system data generator for capturing and generating fiber optic print image data. This board contains a XC4036, DRAM, a PCMCIA flash memory card, a 125Mbit fiber optic link and a 1.2Mbit fiber optic link. This project included the board design and three different FPGA designs.
- ***May 1999 to July 1999*** – **Silver Engineering Inc**., Melbourne FL: Designed a video bus monitor, which takes the video data from a star tracker camera and writes it into a SRAM buffer. The data can then be read and analyzed from an attached PC via a parallel port.

• ***June 1997 to July 1998*** - **Summation Research Inc**., Palm Bay FL: Designed and implemented data path manipulation hardware for a RF demodulator. This product consists of two Xilinx XC4020E and a XC4005E controlling two Harris Viterbi Decoders, interfacing to a PIC microcontroller and receiving data from a ten bit A/D. A total of six designs were implemented which were swapped into the FPGAs depending on the operations to be done on the received data stream.
• ***June 1998 to September 1998*** - **Silver Engineering Inc**., Melbourne FL: Implemented a simulator for satellite communication systems.
• ***March 1998 to May 1998*** – **Southwest Microwave Inc**., Tempe Arizona: Designed an FPGA FIFO and interface for a 50Mbit RF modem.
• ***September 1996 to June 1997*** - **ITCN Inc.** Miamisburg OH: Designed a PC based microprocessor emulator. This product consists of a PCI based card with five Xilinx XC4KE and EX FPGAs, 512K of synchronous static RAM and 16 Meg of synchronous DRAM.
• ***January 1997 to May 1997*** - **Scitex Digital Printing**, Dayton OH: Designed and implemented a card for testing an inkjet printing system board. This contract involved the design of a 5K FPGA, the board design and layout, building ten boards, and integration.
• **Insight Electronics, San Diego CA**: Developed and taught an Advanced Xilinx Training Class and a Reconfigurable Computing Class.
• ***December 1996 to March 1997***- **Scitex Digital Printing**, Dayton OH: Designed and built a data generator for testing inkjet printing systems. This involved a number of FPGA designs, custom software, development of the board and enclosure, along with integration.
• ***July 1996 to present*** – **Xilinx Inc**. San Jose CA: Technical Trainer for FPGA design, Advanced Implementation and PCI Core products.
• ***February 1996 to December 1996*** - **Scitex Digital Printing**, Dayton OH: Added additional functionality to a 50MHZ data conversion card containing a 125 Mbit fiber optic interface doing real time processing on data and level shifting to 150 volts. This involved taking a pin and part locked design, adding 50% more logic and making it run twice as fast. The final design was 95% utilized and ran at 50MHZ.
• ***May 1996 to July 1996*** - **Creative Games International**, N. Smithfield RI: Modification of an existing X3K FPGA printer interface design. The only file available for this design was the .lca file and the design had to be reverse engineered in order to make the change.

ITCN, MIAMISBURG OH

Senior Engineer, November 1995 to February 1996

• Designed a PCI based serial bus emulator and monitor. Board included Xilinx 4000E and 5000 series parts.
• Worked on a 100MHZ microprocessor in-circuit emulator. This board did program trace, statistics, and provided multiple levels of triggering on 32-bit processors, at full system speed.

SCITEX DIGITAL PRINTING, DAYTON OH

Senior Engineer, July 1990 to November 1995

• Designed data systems for high-speed ink jet printing systems. This involved designing numerous high integration boards using Xilinx FPGAs, fiber optics, PALs and microcontrollers.
• Designed a raster image processor for a high-speed label printer. This is a 68040 processor board with 64 Meg of memory and Ethernet, serial, centronics, PCMCIA, and VME interfaces.
• All designs were done to meet UL/CSA/TUV and FCC class B specifications.

HARRIS, GOVERNMENT AEROSPACE SYSTEMS DIVISION, PALM BAY FL

Senior Engineer, September 1988 to June 1990

• Translated to a 1.0 micron process, and optimized, a fault-tolerant RISC processor using Synopsys compiler.
• Inserted test structures into ASICs and verified functionality and 90% fault coverage for military ASICs.

FLORIDA INSTITUTE OF TECHNOLOGY, MELBOURNE FL

Graduate Student; Computer Engineering, September 1987 to June 1990

• Thesis: “A Reconfigurable Hardware Transformation Engine for Computer Graphics Applications”. This was an array of Xilinx FPGAs with dedicated dual port memory acting as a reconfigurable graphics coprocessor for a PC. The example designs done to prove concept were a four by four matrix multiply in hardware, and a Mandelbrot set engine. A custom 3-D graphics package was also developed in C to demonstrate the system.

COMSAT LABS, CLARKSBURG MD

Staff Engineer, July 1986 to September 1987

• Designed dual processor and timing boards for a spread-spectrum satellite communication and position location system. Designed simulation equipment for a spread-spectrum central receiving hub.